SERIAL RADIO FREQUENCY TO BASEBAND INTERFACE
WITH POWER CONTROL

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001]   This application is a continuation-in-part of U.S. Patent Application serial number 10/369,853, titled "Serial Radio Frequency to Baseband Interface with Programmable Clock", filed February 19, 2003.

BACKGROUND OF THE INVENTION

[0002]   1. Field of the Invention

[0003]   This invention relates to an interface for coupling a radio frequency (RF) processing section to a baseband processing section. More specifically, this invention relates to communicating power control messages from the baseband section to the RF section.

[0004]   2. Related Art

[0005]   The worldwide use of wireless devices such as two-way radios, pagers, portable televisions, personal communication system ("PCS"), personal digital assistants ("PDAs") cellular telephones (also known as "mobile phones"), Bluetooth devices, satellite radio receivers and Satellite Positioning Systems ("SPS") such as the Global Positioning System ("GPS"), also known as NAVSTAR, is growing at a rapid pace. Current trends are calling for the incorporation of SPS services into a broad range of electronic devices and systems, including PDAs, cellular telephones, portable computers, automobiles, and the like.

[0006]   At the same time, manufacturers design their devices using very different architectures, spanning a wide variety of processors, frequency references, clock rates, and the like. The manufacturers are also very interested in keeping costs as low as possible while providing as much functionality (including SPS capability) as possible. In particular, architectures which split SPS signal processing between a radio frequency (RF) front end a baseband processing section continue to be popular.

[0007]   For example, SiRF Technology, Inc. of San Jose, CA made popular an SPS chipset that included the GRF1 RF chip and GSP1/LX baseband processing chip. These two devices are described in detail in the SiRFStar® I GPS Architecture GRF1 and GSP1 data sheets. As shown in Figure 1, the RF chip 102 communicated data samples to the baseband chip 104 using differential sign signal lines (labeled SIGN), differential magnitude signal

lines (labeled MAGNITUDE), a GPS clock signal line (labeled GPSCLK), and an acquisition clock signal line (labeled ACQCLK). The baseband chip 104 could communicate with the RF chip 102 in a limited single purpose fashion, namely, by using automatic gain control (AGC) clock, data, and strobe signal lines (labeled AGCCLK, AGCDATA, and AGCSTRB respectively) to provide AGC data to the RF chip 102.

[0008]   More recent SPS signal processing chipset solutions include the SiRFStar® IIe (centered around the GRF2i RF chip and GSP2e baseband chip) and SiRFStar® IIt (centered around the GRF2i RF chip and GSP2t baseband chip) solutions. Both retained the multiple signal lines used to communicate data samples from the RF section to the BB section and the unidirectional communication of AGC information from the baseband section to the RF section. However, the BB section communicated AGC information unidirectionally to the RF chip using a single pulse width modulated output that the RF chip sampled. In other words, the SiRFStar® IIe eliminated the multiple signal line AGC communication path in favor of a single output line.

[0009]   For power control, the RF chip typically included a dedicated power control input, for example, one power control input pin that would enable or disable the majority of the RF chip. Thus, there was little or no ability to exercise detailed control over the power consumed by the RF chip. In other words, when the RF chip was active, so were most of the hardware blocks (e.g., phase locked loops, frequency dividers, digital interface sections, and the like) in the RF chip, whether they were needed at the time or not. As a result, the RF chip would consume greater average power than was otherwise necessary. Particularly when incorporated into a device with limited power reserves, such as a battery operated GPS receiver, excess power consumption was a significant drawback.

[0010]   Therefore, a need exists to overcome the problems noted above and others previously experienced.

SUMMARY

[0011]   The invention provides RF power control messaging, as well as related methods of providing RF power control messaging, over an interface between an RF processing section and a baseband processing section. The interface supports general purpose bi-directional message transmission between the RF processing section and the baseband processing section. The interface further supports transmission of SPS signal samples between the two processing sections without adding undue complexity to the interface.

[0012]   In one implementation, the interface includes a message serial interface and a data serial interface. The data serial interface communicates SPS signal sample data from the RF section to the baseband section. The message serial interface communicates messages, including power control messages, between the RF section and the baseband section.

[0013]   As noted above, a message serial interface communicates power control messages between the processing sections. The message serial interface may include a message-in signal line, a message-out signal line, and a message clock signal line. In some implementations, the message serial interface may also include a slave-select signal line. A power control message may include, for example, multiple power control bits. Each power control bit may specify a power state (e.g., powered-up or powered-down) for pre-determined circuitry in the RF section.

[0014]   The complexity of the data serial interface may be reduced, for example, by using a single data bit signal line to serially carry signal samples from the RF section to the baseband section. The data serial interface may also include a data clock signal line that provides timing for the signal samples. In particular, as an example, the data clock signal line may carry a data clock (that includes rising edges and falling edges) nominally running at 16 fo, where fo = 1.023 MHz, while the data bit signal line may carry a data signal comprising

serially transmitted data bits. In one implementation, a first type of data bit is valid on the rising edge of the data clock and a second type of data bit is valid on the falling edge of the data clock. As an example, the first type of data bit may be a sign bit, while the second type of data bit may be a magnitude bit.

[0015]   Other apparatus, systems, methods, features and advantages of the present invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the present invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE FIGURES

[0016]   The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.   In the figures, like reference numerals designate like parts throughout the different views.

[0017]   Figure 1 shows a prior interface between a GPS RF chip and a baseband chip.

[0018]   Figure 2 illustrates a satellite positioning system receiver that includes an RF processing section coupled to a baseband processing section by an interface that includes a message serial interface and a data serial interface.

[0019]   Figure 3 illustrates a timing diagram that shows the relationship between a data clock and a data signal carried, respectively, on a data clock signal line and a data bit signal line that form the data serial interface shown in Figure 2.

[0020]   Figure 4 illustrates a timing diagram that shows the relationship between a message clock and message data bits carried, respectively, on a message clock signal line and message data bit signal line that form part of the message serial interface shown in Figure 2.

[0021]   Figure 5 shows a method for interfacing an RF processing section and a baseband processing section.

DETAILED DESCRIPTION

[0022]   A typical satellite positioning system ("SPS") system has approximately 12 satellites that may be visible at any one time to a wireless device. As used in this document, SPS means any system utilizing satellites and/or land-based communications devices for providing or enabling the determination of a location of the wireless device on the earth, including, but not limited to: a global positioning system ("GPS") (such as NAVSTAR), GLONASS, LORAN, Shoran, Decca, or TACAN. For the purposes of discussion, specific examples of an interface between a GPS RF processing section and a baseband processing section are described. However, the principles underlying the interface are applicable to interfacing RF processing and baseband processing sections in general.

[0023]   Turning first to Figure 2, that figure shows a receiver 200 of a satellite positioning system. The receiver 200 includes an RF processing section 202 coupled to a baseband processing section 204 using an RF-to-baseband interface 206. The RF processing section 202 receives SPS signals, for example the 1575.42 MHz GPS signal, on the RF input 207.

[0024]   The receiver section 200 may be generally regarded as including an RF front end 224 and a baseband back end 226. The RF front end 224 includes the RF processing section 202 and RF-to-baseband interface 206. The RF front end 224 processes the SPS signals received on the RF input 207 through a sequence of downconversion, automatic gain control, and analog to digital conversion. The baseband back end 226 includes the baseband processing section 204 and RF-to-baseband interface 206. The baseband back end 226 processes (using a microcontroller core, CPU, or other control logic) the sampled data provided by the RF front end 224. The baseband back end 226 communicates the processed data to a digital device (e.g., a digital signal processor, general purpose microcontroller or

CPU, or host PC) using one or more address, data, control, and clock signals that comprise the digital communication interface 222.

[0025] Either or both of the RF front end 224 and baseband back end 226 may be implemented as individual single integrated circuits, for example. Thus, the RF front end 224 may be a single package that includes the RF input 207 (e.g., a particular input pin on the package), RF processing section 202, and interface 206 (e.g., a set of interface pins as described in more detail below). Similarly, the baseband back end 226 may be a single package that includes the baseband processing section 204, interface 206, and digital interface 222. The processing performed by the RF processing section 204 and baseband processing section 204 may be that set forth in more detail in the SiRFStar® I, II, or III chipset data sheets, while the interface 206 is described in more detail below. The SiRFStar® chipsets are available from SiRF Technology, Inc. of San Jose California.

[0026] Although, as shown in Figure 2, the functional division between the RF front end 224 and the baseband backend 226 lends itself to being divided into two separate integrated circuits, many other implementations are possible. As one example, numerous discrete logic and signal processing circuit blocks may implement the RF, baseband, and interface 206 functionality. As additional examples, any of the circuitry underlying the functionality of the RF front end 224 and the baseband back end 226 may be incorporated into a single package (e.g., that encloses multiple integrated circuit dies) or integrated circuit, multiple packages or integrated circuits, or distributed across one or more circuit boards. In these implementations, individual wires, circuit board traces, or VLSI metal or polysilicon layers carry the interface 206 signals between the RF processing circuitry and the baseband processing circuitry.

[0027] Furthermore, any of the circuitry underlying the functionality of the RF front end 224 and the baseband back end 226 may be incorporated, with additional functionality, into a

single package or integrated circuit, multiple packages or integrated circuits, or distributed across one or more circuit boards. As examples, the RF and baseband circuitry may be integrated on a die with digital or analog processing circuitry for cellular telephony, PDA operation, or engine, instrument, or electronics controllers for automobiles. Thus, Figure 2, and the examples given above are not limiting; rather, one of ordinary skill in the art will appreciate that the particular implementation, division of functionality, and packaging of the circuitry that implements the RF processing, baseband processing, and interface 206 may vary widely depending on the application at hand, engineering considerations, cost considerations, and the like.

[0028] The interface 206 includes a message serial interface 208 and a data serial interface 210. The message serial interface 208 provides for serial communication of general purpose messages bi-directionally between the RF section 202 and the baseband section 204. In contrast, the RF section 202 employs the data serial interface 210 to transmit SPS signal samples to the baseband section 204.

[0029] As an initial matter, it is noted that in general, the interface 206 signals shown in Figure 2 are CMOS compatible. In particular, the inputs, for logic one, are above $0.7*Vcc$ V, and, for logic zero, are below $0.3*Vcc$ V. Outputs, for logic one, are above Vcc-0.4 V, and, for logic zero, are below 0.4 V. The input/output pins generally operate in either the 2.5 V or 3.3 V voltage ranges, depending on the desired implementation. The real time clock (RTC) input/output pins may operate at 1.5 V, although they may be designed to tolerate 3.3 V levels if desired. Any of the signals, however, may be adapted to different voltage ratings or specifications depending on the desired implementation.

[0030] The message serial interface 208, as shown in Figure 2, includes the message-in signal line (labeled MSG_DO / MI), a message-out signal line (labeled MSG_DI / MO), a

message clock signal line (MSG_CLK / MK) and a slave-select signal line (labeled MSG_CEB / SS_N[0]). The labels on the message signal lines indicate the direction of data flow from the perspective of the RF section 202 / baseband section 204. For example, the message-out signal line (MSG_DI / MO) carries message bits input to the RF section 202 and output by the baseband section 204.

[0031] The data serial interface 210 includes the data clock signal line (labeled ACQCLK) and the data bit signal line (labeled SGNMAG). The data serial interface 210 generally uses only a single data bit signal line to communicate, serially, data bits to the baseband section 204 (as discussed below in greater detail with regard to Figure 3). Thus, the data serial interface 210 generally includes as few as two signal lines: one for a data clock and one for data bits. The data serial interface 210 is thus a low complexity solution for a SPS signal sample interface between the RF section 202 and the baseband section 204.

[0032] As shown in Figure 2, the receiver section 200, on the RF processing side, also includes a real time clock (RTC) oscillator (OSC) and monitor section 212. A 32 KHz crystal (or other clock source) provides an input clock 214 for the RTC OSC section 212. The RTC OSC section 212 generates a clock output on the RTCLK / RIN signal line that the baseband section 204 uses to keep, as examples, GPS time or UTC time. The clock output is, for example, a 32,768 Hz 1.5 V CMOS output. The RTC OSC section 212 continues to run during power down modes to help the baseband section 204 maintain an accurate timebase.

[0033] However, monitoring circuitry (e.g., a rectifier coupled to the clock input and followed by a comparator) in the RTC OSC section 212 determines when the input clock 214 has consistently run (e.g., has stopped for no more than 10-30 clock cycles). If the clock has stopped for too long, then the RF section 202 sets a bit (e.g., sets a flip/flop output or sets a bit in a multi-bit status register) to indicate that the clock output has not been consistent (and,

in some cases, that the baseband section 204 should search over the full range of the received SPS signal to determine the correct time).

[0034]   The RF section 202 also accepts clocking input from either a crystal oscillator 216 or an external clock source 218 (e.g., a frequency reference provided in a wireless device). The clocking inputs 216 and 218 provide a clock source that a PLL divider chain in the RF section 202 uses to generate the ACQCLK signal. The clocking inputs 216 and 218 are collectively referred to below as the OSCCLK, while the PLL divider chain clock is referred to as the PLLCLK. The PLLCLK is typically set to generate a nominal frequency of 16 fo (where fo = 1.023 MHz) on the data clock ACQCLK derived from the OSCCLK (or an internal reference).

[0035]   At power-up, the OSCCLK (generally in the range of 5 - 27 MHz) is present on the ACQCLK output. A message (described below) commands the RF section 202 to switch ACQCLK from OSCCLK to the PLLCLK and from the PLLCLK to the OSCCLK. The ACQCLK signal may be a 2.5 / 3.3 V CMOS output with a duty cycle between 45% and 55% (except when switching clock sources, in which case ACQCLK may have an extended low cycle).

[0036]   A power control signal (labeled PWRUP / RFPWRUP) may optionally be provided to control whether certain portions of the RF section 202 are powered-up. The power control signal may be connected, for example, to a voltage regulator enable pin in the RF section 202 to provide a coarse power-up / power-down control over the majority of the circuitry in the RF section 202. On the other hand, the RTC OSC section 212 is separately powered so that it can continue to provide a clock to the baseband section 204. The power control signal may be a 2.5 / 3.3 V CMOS signal. The baseband processing side includes an RTC logic section 220. The RTC logic section 220 accepts the input clock generated by the

RTC OSC and monitor section 212 as an aide in determining the current time as well as SPS

location solutions.

[0037]   The RTC logic section 220 also outputs the reset signal GRFRST_N / RESET_N

(asserted low). The reset signal may be used to reset the state of control registers in the RTC

OSC section 212 and the RF section 202 at power-on. For example, when GRFRST_N is

asserted, the digital control registers on the RF processing side will be reset to their default

states. The default states of the control registers allow the OSCCLK circuits to operate and

allow the ACQCLK output to be driven by OCSCLK (when PWRUP) is asserted. When

GRFRST_N is not asserted, then the RF section 202 operates according to its internal logic

states.

[0038]   In one implementation, the message serial interface signals are 2.5 / 3.3V CMOS

I/O signals. The MSG_CLK / MK, MSG_DI / MO, and MSG_CEB / SS_N[0] signals are

inputs to the RF section 202. The MSG_DO / MI signal is an output from the RF section 202

with tri-state control. When the MSG_CEB / SS_N[0] is logic high, the MSG_DO / MI

output is high impedance and may be driven by other devices that are also connected to the

message serial interface 208. Thus, the MSG_CEB / SS_N[0] output from the baseband

section 204 operates as a slave selection signal that allows the RF section 202 to drive data on

the MSG_DO / MI signal line. When additional devices are attached to the message serial

interface 208, the baseband section 204 may provide additional slave selection signal lines to

determine which device is allowed to drive data on the MSG_DO / MI signal line.

[0039]   The RF section 202 may also include one or more inputs for external analog

sensors (not shown). Thus, a multi-channel analog to digital (A/D) converter in the RF

section 202 may take measurements of analog input signals and communicate the results to

the baseband section 204. The analog inputs may include, but not be limited to, temperature

inputs, gyro turn rate inputs, wheel tick inputs, or a battery voltage inputs.

[0040]   Table 1 summarizes the operating modes for the receiver section 200:

Table 1			
Mode	GRFRST_N	PWRUP	Operation
Sleep	0	0	RF section voltage regulator disabled; RTC OSC section isolated from RF section.
Start-up	0	1	RF section voltage regulator enabled; RTC OSC section isolated; registers reset; OSCCLK enabled; ACQCLK outputs OSCCLK.
NA	1	0	Not allowed.
Normal	1	1	RF section voltage regulator enabled; RTC OSC section communicates with RF section; messages control RF section operation.

[0041]   Turning next to Figure 3, that figure illustrates a timing diagram 300 that shows

the relationship between a data clock 302 and a data signal 304. The data signal 304 provides

SPS signal samples to the baseband section 204. The SPS signal samples are derived from an

SPS input signal received by an antenna connected to the RF section 202. The ACQCLK

signal line carries the data clock 302, while the SGNMAG signal line carries the data signal

304. The data signal 304, which may be, for example, a 2.5 / 3.3 V CMOS output, transmits

both sign bit data 306 and magnitude bit data 308 on the SGNMAG signal line. In one

implementation, the data signal 304 provides sign and magnitude bit information determined

by an A/D converter in the RF section 202.

[0042]   In other implementations, additional bits of information or quantization may be

provided, in concert with a predetermined protocol or encoding technique applied to the data

bits (e.g., a pseudorandom noise code) to allow the baseband section 204 to identify the data

transmitted. Furthermore, the data signal 304 may transmit signal samples for different radio chains handled by the RF section 202. For example, when the RF section 202 is processing SPS data, the data signal 304 may bear the two bits per sample (sign and magnitude) data pairs noted above. In contrast, when the RF section 202 is processing a different RF signal (e.g., a Bluetooth signal), the data signal 304 may instead transmit more or less bits per sample (e.g., 4 or 6 bits) in accordance with the guidelines established for processing that RF signal. Similarly, the data clock 302 may vary in frequency and duty cycle to meet the processing guideline for the RF signal that the RF section 202 is currently processing.

[0043] As shown in Figure 3, the RF section 202 outputs the sign bit 306 when the data clock 302 is high and outputs the magnitude bit 308 when the data clock 302 is low. As shown in Figure 3, the sign bit 306 is valid no less than $T_{SETUP-F}$ before the falling edge 310 of the data clock 302. Similarly, the magnitude bit 308 is valid no less than $T_{SETUP-R}$ before the rising edge 312 of the data clock 302.

[0044] The sign bit 306 remains valid no less than T_{HOLD-F} after the falling edge 310 of the data clock 302. The magnitude bit 308 remains valid no less than T_{HOLD-R} after the rising edge 312 of the data clock 302. The setup and hold times may vary from implementation to implementation. As one example, the setup and hold times may be approximately 5 - 10 ns.

[0045] The message serial interface 208 may be implemented in a wide variety of ways. In one implementation, the message serial interface 208 has the characteristics set forth below, although other implementations are also possible.

[0046] The message serial interface on the RF section 202 operates as a slave device to the baseband section 204 (or other master device that adheres to the characteristics set forth below). The inputs bits to the RF section 202 (on the MSG_DI line) are shifted into a 32 bit shift register in the RF section 202 under control of the MSG_CLK. In one implementation,

up to 32 bits are sent in one message block and data is received and transmitted with the most significant bit first. Simultaneously, the MSG_DO output bits are shifted out of the other end of the same shift register. If output from the RF section 202 is not needed, then the MSG_DO output need not be connected. In one implementation, the MSG_CLK operates at up to 20 MHz and the message serial interface signals are, approximately, above 0.8*VCC V for logic 1 and below 0.2*VCC V for logic 0.

[0047]   The slave select signal line (MSG_CEB) is active low for serial data transmission. The MSG_DI and MSG_CLK may therefore be ignored as long as MSG_CEB has been high for a pre-selected period of time (e.g., 5 ns). Data is sampled on the rising edge of MSG_CLK. In one implementation, a transition on MSG_DI or MSG_DO occurs at least 5 ns after the rising edge of MSG_CLK and stabilizes at least 5 ns before the next rising edge of MSG_CLK. The data is shifted on the falling edge of MSG_CLK. Continuing the example, the MSG_CEB signal may be active (logic 0) at least 10 ns before the rising edge of the first MSG_CLK and may remain active (logic 0) at least 10 ns after the last falling edge of MSG_CLK. The time interval in both cases may be, for example, one half of one clock cycle. The MSG_CEB signal may then be held inactive (logic 1) for at least 30 ns to provide time for the RF section 202 to latch the data.

[0048]   If the MSG_CEB signal transitions high before all data in a message block have been sent, the data is discarded and not applied to RF section 202 registers. Unused bits in a message block are set to zero. However, a fast write mode is provided to allow for a shortened, one byte message. The fast write mode is assumed until more than 8 bits have been received. When more than 8 bits have been received, the RF section 202 expects to receive a full 32 bits for a valid message.

[0049]   The RF section 202 outputs data (on MSG_DO) to the baseband section 204 in response to a message received from the baseband section 204 that requests the data. The baseband section 204 then sends a subsequent message to shift out the requested data in the RF section 202 shift register from the shift register. The subsequent message may be an independent operational message or it may be a dummy message sent for the sole purpose of shifting out the desired data.

[0050]   Figure 4 illustrates a timing diagram 400 that shows the relationship between the slave select signal (MSG_CEB) 402, the message clock signal (MSG_CLK) 404, and the message data bit signals (MSG_DO and MSG_DI) 306. Data transmission starts when the slave select signal 402 falls. The transmitted data are latched when the slave select signal 402 rises.

[0051]   As shown in Figure 4, the message-out signal line (MSG_DI / MO) and message-in signal line (MSG_DO / MI) each carry a serial bit stream. The serial bit stream on the message-out signal line represents a message selected from a group of predefined RF section messages that are transmitted from the baseband section 204 to the RF section 202. Similarly, the serial bit stream on the message-in signal line represents a message selected from a group of predefined baseband section messages that are transmitted from the RF section 202 to the baseband section 204.

[0052]   The messages are not limited to any particular purpose or format. As explained in more detail below, the messages may include, but not be limited to, RF section power control messages, RF section test messages, clock status messages, analog measurement messages, channel conversion count messages, and the like.

[0053]   In one implementation, there are four types of message blocks defined. Data [1:0] (in a 32-bit or 8-bit sequence) are address bits that define the four messages as shown in

Table 2 below. Each message type is able to support both a fast write mode and a full write mode and spare capacity has been defined for both modes.

Table 2 - Message Blocks		
Data [1:0]	Message Type	Message Name
00	0	AGC (Fast Write) and Synthesizer
01	1	Power Control (Fast Write) and Synthesizer
10	2	Output Message Types
11	3	Input Message Type Expansion

[0054]   Exemplary contents of each message are shown in detail in Tables 3 through 8. Table 3 shows AGC and synthesizer control messages, Table 4 shows power control and synthesizer control messages, and Table 5 shows output request types for a selected message type. Table 6 shows output message types and Tables 7-8 show input message types, The columns define the contents as follows. The first column, labeled Bits, represents the message data bits, with bit 0 indicating the last bit transmitted. The second column, labeled Field Name, identifies the name of the field in the message. The third column, labeled Length, is the length of the field. The forth column, labeled Default, indicates the contents of the default parameter in the RF section 202 when power is first applied. The fifth column, labeled Contents, describes the allowed contents of the field. The sixth column, labeled Function, indicates what the field accomplishes. The seventh column, labeled _Pwr, indicates which power domain control bit shown in Table 4, if any, is used to drive these field outputs to zero on the interface to the RF section 202.

[0055]   Message type 2 provides for implementing output requests using a field that specifies up to 32 types of output requests. Message type 3 provides for expanding the input message types (or addresses) from 4 to 36. References below to the "synthesizer" are references to the PLL synthesizer clock generation circuitry in the RF section 202. The PLL

synthesizer is configurable, for example, by setting clock divider values to generate the

PLLCLK from a number of different input reference frequencies.

Table 3 – Message Type 0: AGC and Synthesizer Control (Address [1:0] = 0)						
Bits	Field Name	Length	Default	Contents	Function	_Pwr
31:28	Spare0 [3:0]	4	0	0	Spare	
27:8	NUM [19:0]	20	TBD	0x00000 – 0xFFFFF	Specifies the numerator of the fractional part of the loop divider in the PLL clock generation section of the RF section 202.	Synth
7:2	AGC [5:0]	6	0	0x00-0x3F	Controls AGC gain in the RF section 202	Rx
1:0	Address [1:0]	2	0	0	Defines message type	

Table 4 – Message Type 1: Power Control and Synthesizer Control (Address [1:0] = 1)						
Bits	Field Name	Length	Default	Contents	Function	_Pwr
31:28	Spare1 [3:0]	4	0	0	Spare	
27	InvertFePwr	1	0	0: Fe_Pwr = Rx_Pwr 1: Fe_Pwr = ~Rx_Pwr	Partition the reception chain in the RF section 202 for testing purposes	
26	WideBwFilter	1	1	0 = Narrow BW 1 = Wide BW	Select the filter used in the RF section 202.	Rx
25:18	ND [7:0]	8	-	0x00 – 0xFF	Specifies the integer part of a synthesizer loop divider parameter in the PLL clock generation section	Synth
17:15	RDIV [2:0]	3	-	0x0 – 0x7	Specifies a	Synth

Bits	Field Name	Length	Default	Contents	Function	_Pwr
					synthesizer reference divider value in the PLL clock generation section	
14:11	CP [3:0]	4	-	-	Specifies the synthesizer charge pump output and test modes	PLL
10	PD_POL	1	-	1=positive, 0=negative	Specifies the phase detector polarity	PLL
9	DvSel	1	1	0=Fractional 1=Integer	Specifies the divider for PLL feedback	PLL
8	SDO	1	1	0=Third Order SD 1=First Order SD	Chooses Sigma Delta Order	Synth
7	Rx_Pwr	1	0	1=on, 0=off	Controls front end power for 2nd low noise amplifier through A/D converter	
6	AcqClk_Sel	1	0	1= PLL, 0=Osc	Controls glitch-free switch that selects OSCCLK or PLLCLK for ACQCLK	
5	Synth_Pwr	1	0	1=on, 0=off	Controls power to fractional N synthesizer	
4	PLL_Pwr	1	0	1=on, 0=off	Controls power for PLL and divider chain	
3	LNA1_Pwr	1	0	1=on, 0=off	Controls power for first (optional) LNA	
2	Osc_Pwr	1	1	1=on, 0=off	Controls power for oscillator, ACQCLK-select mux and ACQCLK driver	

Table 4 – Message Type 1: Power Control and Synthesizer Control (Address [1:0] = 1)

Table 4 – Message Type 1: Power Control and Synthesizer Control (Address [1:0] = 1)						
Bits	Field Name	Length	Default	Contents	Function	_Pwr
1:0	Address [1:0]	2	1	1	Defines message type	

Table 5 – Message Type 2: Output Request Types 0 to 31 (Address [1:0] = 2)					
Bits	Field Name	Length	Default	Contents	Function
31:8	Spare2 [28:5]	24	0	0	Spare
7:3	Spare2 [4:0] or Out_Dat [4:0]	5	0	0-31	Spare (Fast Write), if Out_Req=0 Output data type, if Out_Req=1
2	Out_Req	1	0	0=data 1=output	When=0, data follows When=1, output data to load follows
1:0	Address [1:0]	2	2	2	Defines message type.

[0056]   Output message types are shown in Table 6. Spare messages have been defined for expansion or use in testing the RF section 202. Since this data is input to the message interface from the RF section 202, these fields are given names denoting input, such as spareInA. When the data is shifted out, it is positioned in the output data stream using the index values given. For example, spareInA [23:0] would be located in the final 24 bits shifted out in the 32 bit output field, so that eight leading zeros would be followed by spareInA [23] through spareInA [0] according to the convention of shifting out the most significant bit first.

[0057]   Out_Dat [4:0] = 4-8 specify 20-bit measurements taken by a dual slope A/D converter in the RF section 202. As noted above, the A/D converter may have multiple channels connected to one or more analog measurement devices. As used below, Out_Dat

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[4:0] = 9 specifies the valid clock bit maintained by the RTC OSC section 212 and described

above.

Table 6 – Output Messages Defined Using Message Type 2 (Address [1:0] = 2 and Out_Req = 1)		
Out_Dat [4:0]	Message Bits	Contents
0	31:24 23:0	0 SpareInA [23:0]
1	31:24 23:0	0 SpareInB [23:0]
2	31:24 23:0	0 SpareInC [23:0]
3	31:24 23:0	0 SpareInD [23:0]
4	 31:30 29:20 19:0	DS_ADC_CH_0 LAST_CH [1:0] Spare [9:0] DATA0 [19:0]
5	 31:30 29:20 19:0	DS_ADC_CH_1 LAST_CH [1:0] Spare [9:0] DATA1 [19:0]
6	 31:30 29:20 19:0	DS_ADC_CH_2 LAST_CH [1:0] Spare [9:0] DATA2 [19:0]
7	 31:30 29:20 19:0	DS_ADC_CH_3 LAST_CH [1:0] Spare [9:0] DATA3 [19:0]
8	 31:30 29:20 19:0	DS_ADC_CNT LAST_CH [1:0] Spare [9:0] COUNT [19:0]
9	 31:1	RTC_STA Spare [30:0]

Table 6 – Output Messages Defined Using Message Type 2 (Address [1:0] = 2 and Out_Req = 1)		
Out_Dat [4:0]	Message Bits	Contents
	0	0=RTC Not Valid (default) 1=RTC Valid
29	31:26 25:0	0 Power Control Message Register [24:0]
30	31:0	Message Input Shift Register
31	31:16 15:0	0 Chip Version [15:0]

Table 7 – Message Type 3: Expanded Input Message Types (Address [1:0] = 3)					
Bits	Field Name	Length	Default	Contents	Function
31:8	Spare3 [28:5]	24	0	0	Spare
7:3	Spare3 [4:0] or Address [6:2]	5	0	0-31	Spare (Fast Write), if Addr_Exp=0 Address expansion, if Addr_Exp=1
2	Addr_Exp	1	0	0=data 1=address	When=0, data follows When=1, address follows
1:0	Address [1:0]	2	3	3	Defines message type.

[0058] Spare messages (useful for test or expansion purposes) are shown in 8. Because these data represent control bits output by the message interface to the RF section 202, the data fields have been named to denote outputs, for example SpareOutA.

[0059] A test message has also been define for the SGNMAG output signal line. When TestSignMag [8] = one, the test mode is entered. When the bit is a zero, test mode is turned off. In test mode, the pattern specified in TestSignMag [7:0] is output, as long as ACQCLK is running, beginning with TestSignMag [7] while ACQCLK is high.

Table 8 – Input Messages using Message Type 3 (Address [1:0] = 3 and Addr_Exp = 1)			
Address [6:2]	Msg Bits	GRFRST_N	Contents
0	31:8	0	SpareOutA [23:0]
1	31:8	0	SpareOutB [23:0]
2	31:8	0	SpareOutC [23:0]
3	31:8	0	SpareOutD [23:0]
4	16:8	0	TestSignMag [8:0]
5			DS_ADC_PER
	31:12	0	PERIOD [19:0]
	11	0	CLK_SEL
	10	0	CLK_ENB
	9:8	0	Spare [1:0]
6			DS_ADC_SH
	31:12	0	SHIFT [19:0]
	11:8	0	Spare [3:0]
7			DS_ADC_PH
	31:12	0	PH_ONE [19:0]
	11:8	0	Spare [3:0]
8			DS_ADC_SEQ
	31:12	0	CH_SEQ [23:0]
	11:8	0	Spare [3:0]
9			RTC_CTL
	31:10	0	Spare [21:0]
	9	0	1: Set RTC Status 0: No action (default)
	8	0	1: Read RTC Status 0: No action (default)
10			SGNMAG_SIG
	31:1	0	Spare [30:0]
	0	0	0: SGNMAG (default) 1: OSCCLK

[0060]   Address [6:2] = 5 - 8 specify parameters for the dual slop A/D converter in the RF

section 202. The DS_ADC_PER message sets the 20-bit conversion period, the duration of an

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entire A/D conversion cycle (PERIOD), selects one of the input clocks (e.g., OSCCLK or PLLCLK) provided to the A/D converter (CLK_SEL), and enables or disables the clock (CLK_ENB). The DS_ADC_SH message provides a 20-bit shift period (SHIFT) that the A/D converter control circuitry uses as a count down value before initiating conversion in order to change the phase of the A/D conversion cycles relative to any given time base. The DS_ADC_PH specifies a 20-bit phase one conversion period (e.g., the duration of the integration period) for the dual slop A/D converter.

[0061]   The DS_ADC_SEQ message specifies 24 bits that control the order in which the A/D converter performs a conversion on each of four input channels. More specifically, the 24 bits are partitioned into 12 pairs of bits; each pair specifies the next input channel to the analog multiplexer before the A/D converter. The pairs of bits thus control which channel is next digitized by the A/D converter and the four input channels may thereby be sampled at different rates.

[0062]   Continuing with regard to Table 8, Address [6:2] = 9 specifies that the clock status bit in the RTC OSC section 212 will be set to indicate a good clock, or (if bit 8 is a one) that the baseband section 204 is requesting the value of the clock status bit to be output by the RF section 202. Address [6:2] = 10 controls (e.g., via a multiplexer) the signal that the RF section 202 provides on the SGNMAG signal line. The default is the sign bit and magnitude bit information, while the alternative is the OSCCLK signal.

[0063]   Bits 2-7 in the message format shown in Table 4 are power control bits. Those bits control whether particular hardware elements in the RF section 202 are powered-up or powered-down. The bits may be transferred from the shift register in the RF section 202 and applied to power control circuits that apply or remove power from specific hardware elements. For example, bit 5, the PLL_Pwr bit, controls power for a phase locked loop (PLL)

circuit and frequency divider in the RF section 202. When the RF section 202 receives a message that has bit 5 cleared, the RF section 202 may remove power from the PLL and divider circuitry by opening a switch through which power flows, driving a power regulator control pin, or through another mechanism. Similarly, when the RF section 202 receives a message that has bit 5 set, the RF section 202 may apply power to the PLL and divider circuitry by closing the switch, enabling the power regulator, or the like.

[0064] While the message format provides five power control bits for (2, 3, 4, 5, and 7), more or fewer power control bits may be provided depending on the implementation. Each bit specifies a power control state (e.g., power-up or power-down) for one or more sections of pre-selected circuitry in the RF section 202. Furthermore, in other implementations, multiple bits may be employed to specify a power state that includes multiple levels of power control. Thus, for example, two bits may be employed to specify one of four different power states for a particular set of circuitry in the RF section 202.

[0065] While Tables 2-8 provide one example of message formats, many other implementations are also possible. Shown below in Tables 9-11 is another exemplary format that employs 56-bit messages without using a 2-bit message block definition.

Table 9 - Message Structure					
Bit # <0:55>	Field Name	Length (bits)	Contents	Function	Default
55	Tst_Ref_Div	1	0 = normal operation 1 = connect reference divider output to test output pin (e.g., scan data output).	Reference divider scan test	0
54	ID_Read	1	0 = normal operation 1 = revision number output to test output pin (e.g., scan data output).	Chip ID read function	0

Bit # <0:55>	Field Name	Length (bits)	Contents	Function	Default
53	IF_TestMux	1	0 = AGC Test Point 1 = Mixer Test Point	Selects either AGC Test Point or Mixer Test Point to TP_IF pin if Mode is set to 11 (IF Test Point Enable).	0
52-29	NUM[23:0]	24	x000000 to xFFFFFF	Numerator of the fractional part of the loop divisor	x898232
28-21	ND[7:0]	8	x00 to xFF	Synthesizer integer part of loop divider	x5A
20-18	SPARE	3	(default)	Not Used	x0
17-14	CP[3:0]	4	See Table 11	Synthesizer Charge pump output current, and test modes	1011
13	PD_POL	1	1 = positive 0 = negative	Phase detector polarity	1
12-11	ACC[1:0]	2	00 = 3 Fractional Accumulators 01 = 2 Fractional Accumulators 10 = Integer Divider, 0 Accumulators 11 = Integer Divider. 0 Accumulators		00
10	SPARE	1	Pad with zeros	Not Used	1
9	CMOS_PEC LB	1	1 = CMOS output buffer selected 0 = PECL output buffer selected	Selects the CMOS or PECL output buffer.	0
8	DIV32_EN	1	1 = enable 0 = disable	Divide by 32 enable	1

Table 9 - Message Structure

Bit # <0:55>	Field Name	Length (bits)	Contents	Function	Default
7	Ref_Osc_EN	1	1 = enable 0 = disable	Power control for the clock oscillator and buffer section in the RF section 202	1

Table 10 - FAST Mode Bits - Power Control

6	RX_Chain_EN	1	1 = enable 0 = disable	Power control for the radio frequency amplifier (RFA), Mixer, AGC amp, and ADC in the RF section 202. Enables ACQCLK, SIGN, and MAG outputs.	1
5	LNA_EN	1	1 = enable 0 = disable	Power control for the LNA Amplifier circuit in the RF section 202.	1
4	CLKGPS_EN	1	1 = enable 0 = disable	Power control for the CLKGPS, and PECL reference if PECL is selected.	1
3	Synth_EN	1	1 = enable 0 = disable	Power control for the Charge Pump, Phase Detector, Prescaler, and Logic in the RF section 202.	1
2	VCO_EN	1	1 = enable 0 = disable	Power control for the VCO circuit in the RF section 202	1
1-0	Mode[1:0]	2	00 = GPS Clock Only Mode 01 = Normal Operating Mode 10 = Standby Mode (Sleep) 11 = IF Test Point Enable	Sets up the operating mode of the RF section 202.	00

Table 11 - Charge Pump Programming Fields				
cp<3>	cp<2>	cp<1>	cp<0>	
1	0	0	0	50 uA, Normal operation of charge pump
1	0	0	1	100 uA, Normal operation of charge pump
1	0	1	0	300 uA, Normal operation of charge pump
1	0	1	1	500 uA, Normal operation of charge pump
1	1	0	0	700 uA, Normal operation of charge pump
1	1	0	1	900 uA, Normal operation of charge pump
0	0	1	1	Test mode: all charge pump outputs source current
0	0	0	1	Test mode: all charge pump outputs sink current
0	1	1	1	Test mode: all charge pump outputs source and sink current simultaneously.

[0066]   Tables 9-11 show an implementation in which the last eight bits of the message are power control bits. Thus, power control may be communicated through a fast message as set forth previously. As noted above, the power control bits determine whether particular hardware elements in the RF section 202 are powered-up or powered-down. The power control bits are not limited to controlling the hardware blocks described in Table 10 (or Table 4). Instead, depending on the implementation, the power control bits may be established in the message to control power to any desired hardware circuitry that will be incorporated into the RF section 202.

[0067]   The baseband section 204 may thereby establish a detailed control over the power consumed by the RF section 202. In other words, the baseband section 204 may determine, at any given time, those hardware blocks in the RF section 202 that will operate, and those that will be powered down. As a result, the RF section 202 will consume less average power than an RF section in which all the hardware blocks operate continuously. Such power control is very useful in battery operated devices, or in any other SPS enabled device with a limited power supply.

[0068]   Turning next to Figure 5, that Figure shows a flow diagram 500 that shows a method for interfacing the RF section 202 and the baseband section 204. In particular, with regard to the serial transmission of SPS signal samples to the baseband section 204, the RF section 202 places a sign bit 306 on the SGNMAG signal line (step 502), then provides a falling edge 310 on the ACQCLK line (step 504). Subsequently, the RF section 202 places a magnitude bit 308 on the SGNMAG signal line (step 506), then provides a rising edge 312 on the ACQCLK line (step 508). This sequence repeats for each sign bit and magnitude bit

sample pair transmitted to the baseband section 204. SPS signal data is thereby serially transferred to the baseband section 204.

[0069]   With regard to message transmission between the RF section 202 and the baseband section 204, the master device (typically the baseband section 204) determines whether it needs to send or receive data over the message serial interface 208 (step 510). If so, the baseband section 204 determines if the message is a fast write message (step 512). If the message is a fast write message, then the baseband section 204 (if it is transmitting data) or the RF section 202 (if it is transmitting data) serially places 8 data bits on the appropriate serial message data line. Each data bit is shifted in by a message clock 404 transition for each data bit. (step 514). Otherwise, the baseband section 204 or the RF section 202 serially places all the data bits (e.g., 32 or 56 data bits) on the appropriate serial message line, with each data bit accompanied by a message clock 404 transition (step 516).

[0070]   The slave select signal line may be used to transfer timing between the baseband section 204 and the RF section 202. In particular, the COUNT[19:0] output (see Table 6, Out_Dat = 8) represents the value of a counter present in the RF section 202 that reveals the sampling phase of the dual slope A/D converter in the RF section 202. The slave select signal line is connected to circuitry in the RF section 202 that latches DSP timing. Thus, the COUNT value is the value in the counter at the time the slave select signal causes the message that requests the COUNT output to latch the COUNT value into the shift register for transmission. In the baseband section 204, the slave select signal latches a counter (or another representation of time) when the slave selected signal is de-asserted (which is also when the RF section 202 latches COUNT).

[0071]   The A/D sample timing may thereby be related to the baseband section 204 timing. The SHIFT[19:0] input (see Table 8, Address = 6) is used to shift the A/D timing to a

desired offset from the baseband section 204 timing. As a result, the baseband section 204 may change the timing of the RF section 202 circuitry without additional interface lines.

[0072] Thus, systems and methods consistent with the invention provide power control messaging (and methods of operating or providing interfaces) between an RF processing section 202 and a baseband processing section 204. The messaging may be employed for many different purposes, and is particularly useful as part of general power control in an SPS device to reduce average power consumption and extend power supply life.

[0073] Typically, powering down as much of the RF section 202 as possible except when taking SPS signal samples helps reduce average power consumption. Taking the samples may in some instances occupy a time span as short as 10-20 ms in strong signal environments outdoors, or 50-100 ms in less favorable conditions outdoors. Indoors, the RF section 202 may operate for a time span on the order of a few seconds to obtain SPS signal samples, particularly for when the signal is weak. Note also that powering down the RF oscillator 212 when the baseband section 204 enters its own power down mode may also reduce power consumption.

[0074] More specifically, an exemplary operational sequence, including power control may proceed as shown below in Table 12:

Table 12	
Operational Step	Description
Initial Powerup	An alarm, timer, or wakeup circuit connected to or incorporated into the RF section 202 or baseband section 204 turns on a power supply connected to the RF section 202 and the baseband section 204.
Baseband Start	The RF oscillator 212 powers up and provides a clock signal to the baseband section 204. The baseband section 204 boots up using the clock signal.
Baseband Initialization	The baseband section 204 performs housekeeping tasks, Input /

	Output initialization, or other processing in preparation for RF section 202 startup.
RF Synthesizer Startup	The baseband section 204 powers up the RF clock synthesizer in the RF section 202 and waits a pre-determined time for the RF clock synthesizer to stabilize.
RF Circuitry Startup	The baseband section 204 turns on power to the LNA, AGC, A/D, and other selected circuitry in the RF section 202 and waits a pre-determined time for those sections to stabilize.
Sampling	The baseband section 204 starts taking data samples from the RF section 202.
Storage	In some modes of operation, the baseband section 204 directs storage of a block of data samples obtained from the RF section 202.
RF Circuitry Shutdown	The baseband section 204 turns off the LNA, AGC, A/D and RF clock synthesizer circuitry in the RF section 202.
GPS Measurement	The baseband section 204 directs processing of the stored data samples in order to extract GPS measurements from the data samples.
Location Update	The baseband section 204 determines a position update and delivers the update to a recipient over an Input / Output interface.
Wakeup Programming	The baseband section 204 programs the timer, alarm, or wakeup circuit for the next wake up alarm and begins shutdown.
Shutdown	The baseband section 204 initiates shutdown, gates off clocks, and powers down the RF section 202 and the baseband section 204 (except for the wakeup alarm circuitry).

[0075]   The foregoing description of the preferred implementations of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention not be limited by this detailed description.